Applicant's invention relates to a matrix type light modulation device which uses a driving ferroelectric gate field effect transistor. Applicant would emphasize that conventional light modulation devices, such as that illustrated in Fig. 1, require a charging time to obtain an electric charge in writing data and to ensure a stable response of the liquid crystal element. To reduce the writing time, a memory element may be used in the matrix. However, the use of the memory device requires the introduction of several transistors into the light modulation device thereby increasing the expense and size of the apparatus.

Applicant's invention is illustrated by example in Fig. 7. The matrix includes a driving circuit comprising a ferroelectric gate field effect transistor. Due to a hysteresis effect in the ferroelectric gate transistor, in a certain gate voltage range for Vgs, a conducting state or a non-conducting state is formed between the source and the drain depending upon the polarization of the ferroelectric substance. The ferroelectric gate FET thus acts as a memory transistor to help increase the writing speed without the additional memory element.

Turning to the cited art, Takahara relates to a display device having the matrix and drive circuit arrangement illustrated in Fig. 1 of the reference. The arrangement essentially corresponds to that of Fig. 1 of the application which illustrates an FET driving device, and in particular a thin film transistor as a drive device. In a description of the operation of the circuit, the thin film transistor comprises a basic switch (See Fig. 18, element S2). Therefore, Takahara suffers the same deficiencies as the conventional device requiring a large stabilizing and write time. The principal object of the reference is to provide a sufficient electric field to effect the orientation of particles in a liquid display element, even if the liquid crystal is very thick. To achieve this, opposite polarities of voltage are applied to each of a pixel electrode and counter

electrode which are disposed on opposite surfaces of the liquid crystal layer. The reference does not disclose a ferroelectric liquid crystal as the Examiner contends, but a PDLC (polymer dispersion liquid crystal).

Okumura generally relates to a display device (TN-crystal type) that relies on small incremental changes in voltages to emphasize the transitions in pixels when an image changes. When a selecting TFT switch 14-1 is turned off, the feed-through voltage ΔVg is applied to a pixel electrode through a capacitance Cgs between the gate and the source. Thereafter, a corrective force is applied to a storage capacitor Cs. Col. 7, line 66 to col. 8, line 7. The corrective voltage is applied via a control line 13-1. Col. 8, lines 38-48. In the TN crystal, a positive voltage to the pixel electrode when the liquid crystal has a positive dielectric anisotropy, and a negative voltage is applied to the pixel electrode when the liquid crystal has a negative dielectric anisotropy.

The Examiner maintains that the combination of Takahara and Okumura teaches or suggests each feature of independent claims 2, 4-6, 8 and 10-11. The Examiner's rejection of the independent claims over Takahara and Okumura is not supportable. Each of the independent claims describes a drive circuit with a ferroelectric gate field-effect transistor, with the ferroelectric gate field effect transistor being provided per pixel. The Examiner's analysis relative to Takahara at page 2, paragraph 3, lines 3-11 does not indicate where the primary reference even teaches such a ferroelectric gate field effect transistor. Because the corresponding schematic description of Takahara, such as Fig. 18, depicts the thin film transistor as a simple switch, this further confirms that the transistor is not a ferroelectric gate transistor. Moreover,

Takahara indicates that a benefit of the reference is the use of conventional transistors. Col. 14, lines 44-50. Therefore, the transistors of Takahara are not ferroelectric gate field effect transistors. The Examiner's citation to elements 104, 105 at page 3, line 4 of the Office Action to correspond to ferroelectric gate field effect transistors is improper. The elements 104, 105 of Takahara correspond to a control circuit and an LC panel (See Fig. 13), not to the transistors specified by the claims. Additionally, the Examiner's reliance on changes to polarization states of a liquid crystal is misplaced. To the extent that Applicant's claims describe a polarization state (claim 12), the polarization relates to a gate of the ferroelectric FET and not the liquid crystal element. Significantly, Takahara does not teach a ferroelectric liquid crystal.

Similarly, Okumura does not teach a ferroelectric gate transistor but a simple thin film transistor. Therefore, the prior art rejection over Takahara and Okumura should be withdrawn.

Applicant would also assert that the references cannot be combined. Whereas Takahara relates to a large potential difference to be applied between a counter electrode and a pixel electrode, Okumura relies on small incremental changes. The references are directed to different objects such that one skilled in the art would not combine their teachings. The references also relate to different display types. In particular Takahara relates to a PDLC display and Okumura relates to a TN liquid crystal. One skilled in the art would not combine the teachings of theses references on this basis.

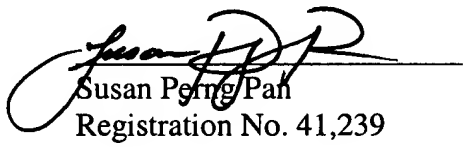
Applicant would further maintain that the Examiner has failed to indicate the equivalence of a binary static drive device as described in the claims and any structure in the art of record. Therefore, claims 6 and 14 are patentable for this additional reason.

With further regard to claims 28-34, the Examiner concedes that a second ferroelectric gate transistor is not taught by the references. The Examiner contends that it would be obvious to include such a second ferroelectric gate field effect transistor for the sake of having a separate ferroelectric element. The Examiner's rationale lacks any basis especially since the references clearly do not even teach the first ferroelectric gate FET. Moreover, the inclusion of the second ferroelectric FET would not further require the connection of data lines described in dependent claims 28-34. Claims 28-34 are patentable for this additional reason.

In view of the above, Applicant submits that claims 2-6, 8-16 and 18-34 are in condition for allowance. Therefore it is respectfully requested that the subject application be passed to issue at the earliest possible time. The Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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